Remarks

The foregoing amendments and following remarks are responsive to the March 28, 2005 Office Action. Applicants respectfully request reconsideration.

Status of the Claims

Claims 1-4, 6-13, 16 and 21 are amended. Claims 1-23 are pending.

Amendments to the Specification

The specification is amended to claim priority to prior applications. No new matter is added.

Amendments to the Drawings

Figures 3A and 3B are amended to correctly identify the first and second circuit conductors. Support for the proposed amendments is found on page 19, lines 3-14 of the specification. Enclosed are copies of the Figures indicating the changes in red ink, and two (2) Replacement Sheets. Approval and entry is respectfully requested.

Support for Amended Claims

Support for the amended claims is found throughout the specification, and particularly on page 2, lines 2-7, page 3, lines 1-6, page 6, lines 4-13, page 7, lines 16-31, page 8, lines 4-12 and lines 29-31, page 11, lines 20-32, page 12, lines 19-21, page 15, lines 21-33, and the Figures. No new matter is added.

Rejection under 35 U.S.C. § 102(e)

Claims 1-5, 7-9, 11-15, 17-20 and 22 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,395,996 to Tsai (the Tsai Patent). Claim 1 (from which Claims 2-5 and 7-9 depend) and Claim 11 (from which Claims 12-15, 17-20 and 22 depend) are amended to clarify the invention.

The Tsai patent relates to a multi-layered substrate with a built-in capacitor. The multi-layer substrate (first, second and third dielectric layers 145, 135, and 125, respectively) includes via holes (105) drilled through the assembled substrate. After via holes are drilled through the substrate, the assembled substrate is separated, and the second dielectric layer (135) is drilled to include a plurality of holes (108). The holes (108) are filled with a high dielectric constant material to adjust capacitance.

According to an aspect of Applicants' invention, a capacitor is embedded in at least one innerlayer panel of a printed wiring board. The capacitor includes a first electrode formed from a foil and having a first electrode termination coupled to the first circuit conductor, wherein the first electrode termination is within the footprint of the first electrode; at least one dielectric layer comprising a high dielectric constant material disposed over the first electrode including an aperture formed therethrough; and a second electrode formed over the first dielectric layer and having a second electrode termination coupled to the second circuit conductor, wherein the second electrode termination is spaced a selected distance from the first electrode termination to reduce separation between terminations.

As described in the specification on page 1, line 23 to page 2, line 7, and on page 2, line 20 to page 3, line 11, a capacitor may contribute to circuit loop inductance through self-inductance and by the degree of termination separation. According to an aspect of the invention, the capacitor includes at least one electrode termination that is within the footprint of the electrode. According to another aspect, locating a second electrode termination within the footprint of the second electrode allows for further reduction of termination separation.

The term "footprint" is common in electronics and typically describes the area and shape of a component that will be placed on the printed wiring board. The phrase "within the footprint of the electrode" thus means that it is within the area and shape of the electrode area covering the high capacitance dielectric. Thus, without having to locate terminations at opposite ends of a capacitor (maximum separation leading to high loop inductances) the invention provides that at least one of the electrode terminations is within the footprint of an electrode, thereby reducing separation between terminations, and leading to lower inductance.

The Tsai patent fails to disclose a first electrode termination being within the footprint of the first electrode; at least one dielectric layer comprising a high dielectric constant material disposed over the first electrode including an aperture formed therethrough; and a second electrode termination being spaced a selected distance from the first electrode termination to reduce separation between terminations. Since the Tsai patent fails to disclose each and every element as claimed, the rejection should be withdrawn.

Rejections under 35 U.S.C. § 103(a)

Claims 6, 10, 16, 21 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Tsai Patent. The arguments set forth above with regard to the rejection under 35 U.S.C. § 102(e) based on the Tsai patent are reasserted herein as if set forth at length.

The Examiner has alleged that plates 130A and 140A are first and second electrodes, respectively. In contrast, element numbers 140A and 130A are conductive trace layers that serve merely to connect the high capacitance capacitor (the high K material in hole 108) to vias 105 as described in column 4, lines 11-13 and 39-41 of the Tsai patent. Conductive layers 139 are formed on conductive trace layers 130A and 140A to form parallel capacitor plates.

As discussed above, the multi-layer substrate of the Tsai patent includes a second dielectric layer (135) with holes (108) drilled therein for built-in capacitor formation. The Tsai patent does not have a dielectric layer comprising a high dielectric constant material with an aperture formed therethrough. Instead, the Tsai patent drills a hole in a dielectric layer and fills the hole with a high dielectric constant material.

The Tsai patent fails to teach, suggest, or provide motivation to include 1) a first electrode termination being within the footprint of the first electrode; or 2) at least one dielectric layer comprising a high dielectric constant material disposed over the first electrode including an aperture formed therethrough; or 3) a second electrode termination spaced a selected distance from the first electrode termination to reduce separation between terminations.

The Examiner's suggestion that it would have been obvious to one or ordinary skill in the art to form a second built in capacitor having a third electrode would not reach the invention as claimed for reasons set forth above. In addition, there is no motivation provided by the Tsai patent to reduce separation between terminations as claimed. If one had the foresight to do as suggested by the Examiner, one still would not be led to the invention as claimed, because there is no teaching or suggestion whatsoever in the Tsai patent to reduce separation between terminations as claimed. In view of the foregoing, reconsideration and withdrawal of the rejections is respectfully requested.

Cited References

The cited references made of record but not relied upon by the Examiner on page 7 of the Action have been considered, and a detailed discussion appears unnecessary.

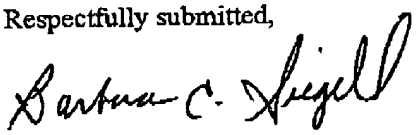
Fees

A fee accompanying the Petition for a One-Month Extension of Time is enclosed. No additional fees are believed due. The Commissioner is authorized, however, to charge (or credit any balance) any fees deemed due (or owing) to Deposit Account 04-1928 (E. I. du Pont de Nemours and Company).

Conclusion

It is respectfully submitted that Claims 1-23 are in condition for allowance. A Notice of Allowance is respectfully requested. If anything further is needed to advance allowance of this application, the Examiner is urged to contact Applicants' attorney at the telephone number below.

Respectfully submitted,



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